

What is claimed is:

1. A method of making a flash memory cell comprising the steps of:
 - forming a first polysilicon layer, which has a bottom surface and a top surface, overlying a substrate with a tunnel oxide layer
 - 5 interposed between the substrate and the first polysilicon layer;
 - forming a trench through the first polysilicon layer, and into the substrate;
 - forming a field oxide layer, having an upper surface, overlying the substrate to a thickness such that the upper surface of the
 - 10 field oxide layer within the trench is higher than the bottom surface of the first polysilicon layer;
 - depositing a second polysilicon layer, having an upper surface, overlying the insulating layer to a thickness such that the upper surface of the second polysilicon layer within the trench is lower than the
 - 15 top surface of the first polysilicon layer;
 - depositing a sacrificial oxide layer over the second polysilicon layer;
 - planarizing the second polysilicon layer, the field oxide layer, and the first polysilicon layer; and
 - 20 stopping the step of planarizing at the top surface of the first polysilicon layer and the upper surface of the second polysilicon layer;
 - depositing a high-k dielectric material overlying the second polysilicon layer; and
 - depositing a third polysilicon layer overlying the high-k
 - 25 dielectric material.

2. The method of claim 1, wherein the field oxide layer is formed by growing a thin thermal oxide and then depositing the remainder of the oxide using a CVD process, or sputtering.

3. The method of claim 1, wherein the tunnel oxide layer is silicon dioxide.

4. The method of claim 1, wherein the high-k dielectric material is hafnium oxide or zirconium oxide.

5. The method of claim 3, further comprising the steps of: depositing and patterning photoresist to define a gate structure;

selectively etching the third polysilicon layer, the high-k dielectric material, the second polysilicon layer, and the first polysilicon layer; and

stopping after the removal of exposed regions of the second polysilicon layer, whereby a thin layer of exposed first polysilicon layer remains.

6. The method of claim 5, further comprising the step of selectively etching the remaining exposed first polysilicon layer using a highly selective etch, whereby the remaining exposed first polysilicon layer is removed without excess removal of the underlying tunnel oxide layer.

7. The method of claim 1, further comprising applying and patterning photoresist overlying the high-k dielectric material prior to depositing the third polysilicon layer; and removing high-k material from areas where non-memory transistors are to be formed.

10 8. The method of claim 7, further comprising depositing a sacrificial polysilicon layer over the high-k dielectric material prior to applying and patterning the photoresist; and removing the sacrificial polysilicon layer from areas where non-memory transistors are to be formed.

15 9. A flash memory cell structure comprising a tunnel oxide overlying a substrate, a floating polysilicon gate overlying the tunnel oxide, a high-k dielectric layer overlying the floating polysilicon gate, and a control gate overlying the high-k dielectric layer.

10. The flash memory cell structure of claim 9, wherein
20 the high-k dielectric layer is hafnium oxide or zirconium oxide.

11. The flash memory cell structure of claim 9, further comprising a source region and a drain region separated from each other by the gate stack comprising the tunnel oxide, the floating polysilicon gate, the high-k dielectric layer and the control gate.